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A Double Quadratic Buck Converter

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Abstract: The Double Quadratic Buck Converter is a new non-insulated DC-DC converter. This new converter is characterized by average output voltage to be lower than input voltage, and the voltage intermediate capacitor also to be lower than the input voltage. It has the advantages of high gain ratio near half range of duty cycle compared to the conventional Buck Converter. In this case, the voltage at the switches is lower than the input voltage and half the voltage in the switch of the existing Quadratic Buck Converter. That means in double quadratic buck converter, the stress voltage over the switches is reduced to half of the value compared to the conventional Quadratic Buck Converter. The topological symmetry simplifies the theoretical analysis of the converter .The converter operation stages with the respective waveforms are explained and closed loop simulation of the new converter is done.

Keywords: Quadratic Buck Converter, Direct current, Continuous conduction Mode, Double quadratic buck converter.

I. INTRODUCTION

1.1 General Background

DC-DC converters are commonly used to provide a stable voltage supply in modem electronic systems. Basic converters that perform a step-down and step-up function are a buck converter and boost converter respectively. In theory, a voltage conversion ratio of these converters depends on a duty cycle of their power switch, ranging between zero and one for the buck converter and between one and infinity for the boost converter. However, in practice, the conversion ratio is often restricted to not more than tenfold because, at this conversion level, the duty cycle is quite small. For example, to attain a step down of 10-to-1 ratio, the buck converter will have to operate with a duty cycle of 0.1. This translates to a control circuit must generate a gate drive signal having narrow pulses, which is prone to be disrupted by the EMI, Moreover, at high switching frequency, the small duty cycle means a short conduction time for a power switch. Under such the short conduction time, the power switch may not operate correctly, as the switch itself has a finite turn-on and tum-off times. To extend the conversion ratio without lowering the duty cycle, N-stage cascade DC-DC converters with one active switch have been recently proposed. The quadratic buck converter whose conversion ratio equals square of the duty cycle, is a special case of the cascade converter, where N is equal to two.

1.2 Relevance

The actual tendencies in industry reveal the idea to use different converters suited for each special application. Hence we will need some converters with special characteristics according to the application type. These imply to identify properties, to classify them and, finally, synthesize the new topologies. The Double Quadratic Buck Converter is a new non-insulated DC-DC converter. This new converter is characterized by average output voltage to be lower than input voltage, and the voltage intermediate capacitor also to be lower than the input voltage. It has the advantages of high gain ratio near half range of duty cycle compared to the conventional Buck Converter. In this case, the voltage at the switches is lower than the input voltage and half the voltage in the switch of the existing Quadratic Buck Converter.

That means in double quadratic buck converter, the stress voltage over the switches is reduced to half of the value compared to the conventional Quadratic Buck Converter. The topological symmetry simplifies the theoretical analysis of the converter.

1.3 Objective

The main goal of this project is to overcome the drawbacks of the conventional buck and quadratic buck converters but preserve the advantages. The double quadratic buck converter has the advantages of high gain ratio near half range of duty cycle compared to the conventional Buck Converter. In this case, the voltage at the switches is lower than the input voltage and half the voltage in the switch of the existing Quadratic Buck Converter. That means in double quadratic buck converter, the stress voltage over the switches is reduced to half of the value compared to the conventional Quadratic Buck Converter.

1.4Organization of the report

Chapter 2: This chapter includes the literature review of related topics of this project. It includes a review of the common techniques used for high step-down dc-dc voltage conversion.

Chapter 3: This chapter focuses on the study double quadratic buck converter.

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Chapter 4: It includes the simulation models of the proposed converter and results.
Chapter 5: It deals with the hardware setup and explanations of various components used for implementing the system. It also provides experimental validation of the results.
Chapter 6: This chapter is the conclusion part and it includes the contributions presented in this thesis.

II. LITERATURE SURVEY

2.1 Introduction

This chapter includes a review of the common techniques used for high step-down dc-dc voltage conversion. First, the limitations of conventional buck & synchronous rectifier buck converters used for high step down dc-dc voltage conversion which include narrow duty cycle, high voltage stress, large ripple and low efficiency are briefly discussed. Then various topologies of non-isolated step-down dc-dc converters are reviewed and discussed. Several applications require high step down voltage conversion.

Some of the most common applications are light emitting diode lamps, voltage regulator modules for microprocessors, telecom equipment and battery operated portable devices such as personal digital assistant, cellular phones and global positioning system etc. For such applications a step down voltage conversion ratio of around 0.1 or even less is required as these applications requires very low dc voltages. Conversely they operate at very high currents.

2.2 Literature survey

2.2.1 Conventional buck converter

The most basic converters used for such type of voltage conversion is a basic buck converter. A basic buck converters and synchronous buck converter are show in Figures 2.1 and 2.2 .This basic step-down dc-dc converter is not suitable for high step down voltage conversion as it must operate at a very small duty ratio ($D=V_O/V_{in}$). Such a small duty ratio effects the dynamic performance of the converter and cause asymmetry in the on and off times of the switches. Moreover extremely small duty ratio limits the converters switching frequency and results in severe reverse recovery problem of free-wheeling diode which degrades the converter's efficiency.

In a conventional buck & synchronous buck converter with high input & low output voltages, there is a very high voltage drop (voltage stress) across the semiconductor switches. This high voltage stress of switches is also a major concern as it increases the ratings of the devices which results in increased size and also increase the switching losses which lowers the converter's efficiency Another issue related with conventional buck & synchronous buck converters is the large current ripples. These large current ripples results in an increase in conduction losses and lowers the overall efficiency of the converter. Large filter inductors must be used to reduce these current ripples which increase the size and weight of the converter .The conventional buck & synchronous buck converter is not suitable for high step down dc-dc voltage conversion due to its several limitations discussed above. A lot of research has been done on DC-DC converters with high step down voltage gain and a number of methods/topologies have been proposed in the literature to obtain a low voltage conversion ratio without the use of small duty ratios, to lowers the switch voltage stress, to decrease ripples and improve efficiency. No review of these step-down dc-dc converter topologies is available in the literature. The aim of this paper is to review the topologies used for high step down voltage conversion and point out the merits and demerits of each. The techniques/methods used for step-down voltage conversion in the literature are divided into different sub groups and then each sub groups is briefly discussed.

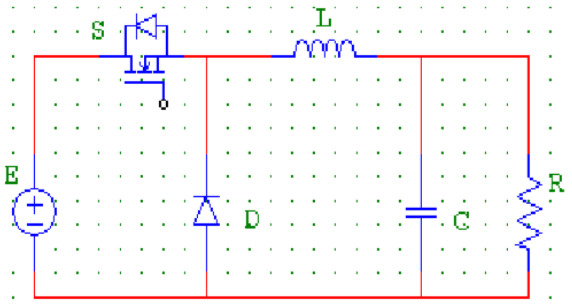

Fig.2.1. Conventional buck converter

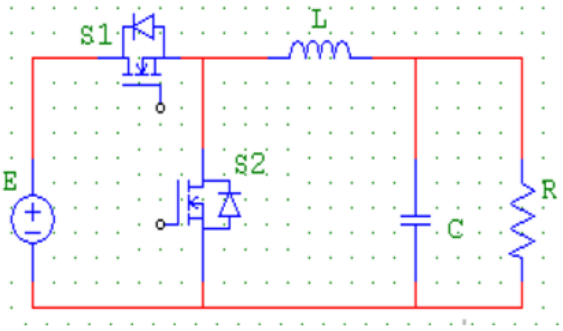

Fig.2.2 synchronous buck converter

2.2.2 Interleaved Buck Converters

To solve the problems of large current ripples associated with conventional buck converters, interleaved buck converter are used by connecting two or more buck converters in parallel. Interleaving technique not only reduces output current ripples but also increase the power ratings .Figure 2.3 shows the circuit diagram of a two phase interleaved buck converter. This converter uses two same inductors in two parallel phases. There are four states of operation in one switching period and during state-I and state-III, when current in one phase increases the current in the other phase decreases and there is a ripple cancellation effect which results in small output current ripples. The current is shared among the two phase

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which decrease the conduction losses and improve efficiency and can be used in high power ratings. However, this topology does not lowers the voltage conversion ratio and still suffer from small duty ratio operation for high step down voltage conversion. The voltage gain of a simple buck and interleaved buck converter is same.

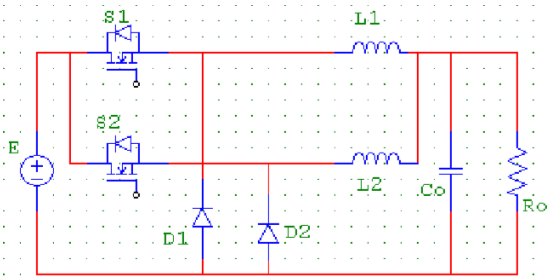

Fig.2.3. Interleaved Buck Converters

Interleaved buck converters with extended duty cycle have been proposed for high step-down voltage conversion. Figure 2.4 shows the circuit diagram of a two phase buck converter with extended duty cycle. One additional input capacitor is used between the two phases for extending the duty cycle and also clamping the voltage stress of switches. The concept can be generalized to more than two phase.

This topology can perform a high step down voltage conversion along with ripples cancellation feature of simple interleaved buck converter. However, it is not suitable for very high step down applications as it only doubles the duty cycle. Moreover, main switch of phase 2 still suffers from high voltage stress.

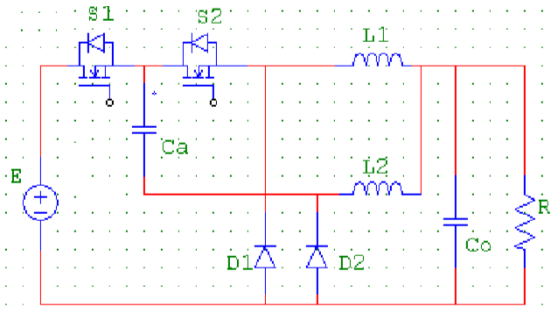

Fig.2.4.Interleaved Buck Converter with Extended Duty Cycle

A modified form of interleaved buck converters with extended duty cycle is shown in Figure 2.5. This structure use three additional capacitors and two additional transistors to lowers the voltage conversion ratio and obtain a large step down voltage gain. This topology is good for high step down conversion as it uses only a two phase interleaved structure and extended the duty cycle four times and also reduce the stress of semiconductor switches to one fourth of the input voltage. The use of more numbers of active switches and capacitors can be a concern as it can increase cost and size.

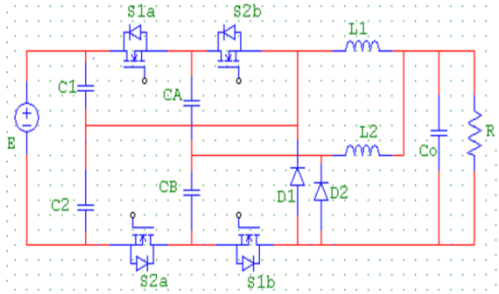

Fig.2.5. Modified Interleaved Buck Converter with Extended Duty Cycle

2.2.3. Quadratic Buck Converters

Quadratic converters are also used for obtaining low voltage conversion ratios. The circuit diagram of a quadratic buck converter is shown in Figure 2.6. This converter uses two buck converters connected in series but employs only one transistor switch. The quadratic buck converter in CCM operates with two circuit states in one switching period. The first state is when S is turned on). During this interval (dT), the inductor L_l and L_2 are in a charging phase, and hence i_{Ll} and i_{Ll} increase linearly. The second state is when S is turned off. During this interval ((1-d)T), L_l and L_2 are in a discharging phase, and thus i_{Ll} and i_{Ll} decreases linearly.

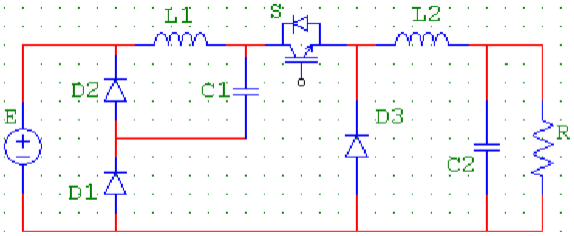

Fig.2.6. Quadratic Buck Converter

This is a good method for high step-down voltage conversion as it gives a quadratic step down conversion ratio which is equal to the product of the conversion ratios of the two single buck converters. The efficiency is also good as it uses only one active switch. The voltage stress across the switches is high.

2.3 Conclusion

The topologies/techniques used for high step down dc-dc conversion are divided into various groups which include interleaved, quadratic etc. Each group of converters is briefly discussed, main circuit structure of each topology is given and their features and limitations are given. To overcome the drawbacks of the aforementioned converters, but preserve their advantages, an effective topology is required. The double quadratic buck converter has the advantages of high gain ratio near half range of duty cycle compared to the conventional Buck Converter. The stress voltage over the switches is reduced to half of the value compared to the conventional quadratic buck converter.

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This paper is organized as follows: chapter 4 gives the general topology of basic HBC and discusses the operation principal. The steady-state analysis is given in Section 5. Circuit performance analysis such as components stress, voltage ripple and circuit comparison are presented in Section 6. Simulation and experimental results are given in Section 7 and the conclusion is drawn in Section 8.

III. DOUBLE QUADRATIC BUCK CONVERTER

3.1 Introduction

Regarding the dc-dc power conversion, robustness, efficiency and low cost with topological simplicity are the main concern. In this perspective, Buck and derived converters are the first converter group to look after. Thus, new topologies derived from the Buck Converter have been investigated in several works. New converter topologies were developed by combining existing converters. The association of the cascade converters, also called converters with more than one stage, originated quadratic converters. Conversion range can be extended significantly if conversion ratio has a quadratic dependence of static gain. Relating to the initial studies of dc-dc converters with cascaded association, the Cuk Converter with two stages, a cell switching responsible for generating a family of dc-dc converters, where originated the analysis to the development of the Quadratic Buck Converter. Whereas the utilization factor of the switch of the Conventional Buck Converter is optimized for high values of duty cycle, namely, low conversion rate static, in applications requiring wide range of the static conversion the Double Quadratic Buck Converter becomes interesting. In this case, a wide range allows the static converter operate with duty cycle suitable for the same voltage applied to the Buck converter Conventional. In this context, this converter can be used in various applications related the use of batteries with a voltage lower than the voltage generating source, such as for example in systems generation photo voltaic , battery chargers for cell phones and switching power supplies, among others.

The Double Quadratic Buck Converter is characterized by average output voltage to be lower than input voltage, and the voltage intermediate capacitor also to be lower than the input voltage. Furthermore, it has high gain ratio compared to the conventional Buck Converter. In this case, the voltage at the switches is lower than the input voltage and half the voltage in the switch of the Quadratic Buck Converter existing in the literature.

3.2. Operating principle

Likewise that the Buck Converter Conventional the Double Buck Quadratic Converter also has step-down voltage characteristic, that is, the output voltage is lower than the input voltage. However, by having high static gain has wide range in the output voltage. In this structure, both the power supply and the intermediate capacitor will behave as voltage source. The load should behave as a current source and the current on the intermediate capacitor is given by the difference between the current across the inductor L1 and the current in the switch S1. Because of its symmetrical topology, the lower components have the same behaviour of the respective upper component. TheFig.3.1shows the topology of the Proposed Converter.

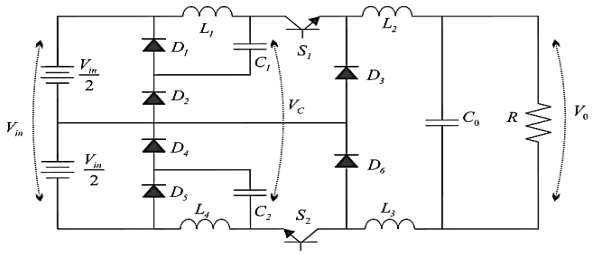

Fig.3.1. Double Quadratic Buck Converter

3.3 Operating Stages

3.3.1 First Stage: (D.Ts)

In this stage the switches S_1 and S_2 are turn on. The diodes D_3 and D_6 are inversely polarized, the current sources I_{L1} and I_{L2}, start to deliver power to the output. The current i_{S1} is the sum of I_{L1} with I_{C1}, and the current i_{D1} is null, Fig. 3.2 shows the first stage operation of double quadratic buck converter.

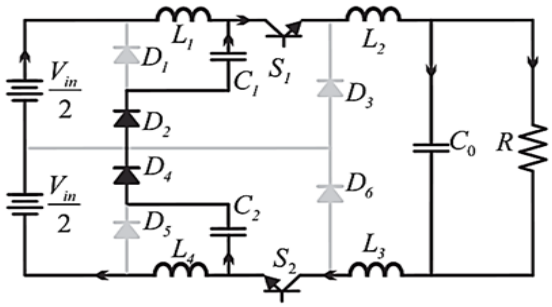

Fig.3.2. First Stage of Operation

3.3.2 Second Stage: ((1−D).T_s)

In this stage the switches $S_1$and S_2 are turn off. The diodes D_3 and D_6 come into conduction, isolating the current source I_{L1} of the output and of the current source I_{L2}. In this stage, the current i_{S1}, i_{S2}, i_{D2} and i_{D4} are nulls, $i_{D1} = I_{L1}$ and $i_{D3} = I_{L2}$, Fig.3.3 shows the second stage of operation of double quadratic buck converter.

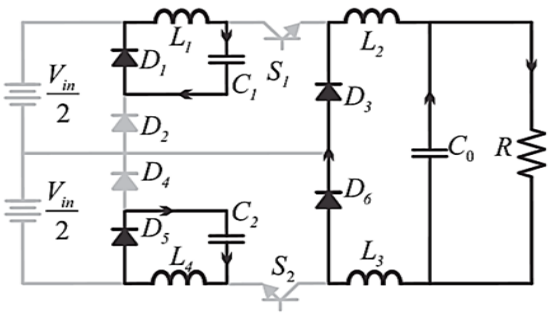

Fig 3.3.Second Stage of Operation

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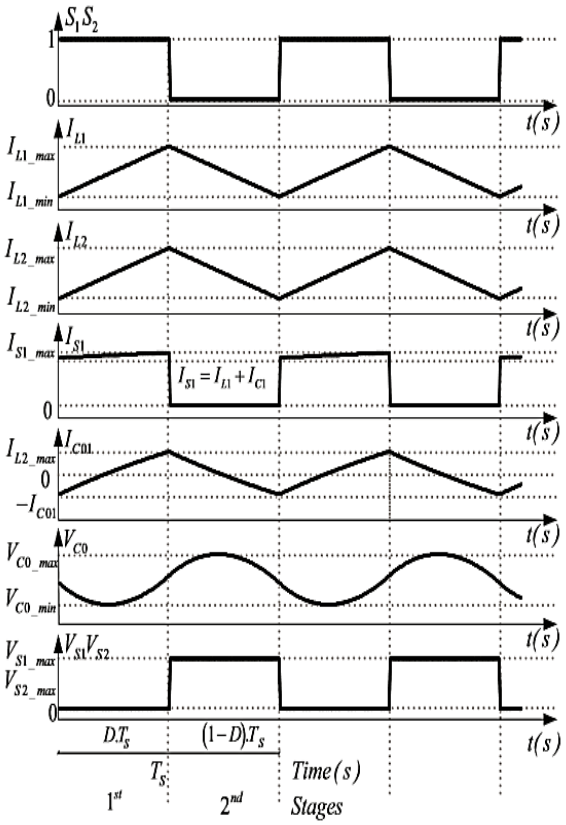

Fig 3.4.Key waveforms of the converter

3.4 Analysis

To draw the curve of ideal static gain, it is considered the energy given by the source Vin in an operation period qual to (3.1).

$$W_{in}=(\frac{Vc}{2}-\frac{Vin}{2}).I_{L1}.\Delta t_1 \qquad (3.1)$$

The energy received by the intermediate capacitors C_1 and C_2 in an operation period is given by (3.2).

$$W_{c1.2} = -\frac{Vc}{2}I_{L1}\ \Delta t_2 \qquad (3.2)$$

Consider in gain deal system, in a period of operation all energy given by the source V_{in} is received by the intermediate capacitors C_1 and C_2. Thus, from equating (3.1) and (3.2) we obtain the Equation of Ideal Static Gain for the first part of the converter, as shown in (3.3)

$$\frac{Vc}{Vin} = D \qquad (3.3)$$

The same analysis is performed for the second part of the converter, considering V_C as the source of input and I_{L2} as the constant current source. Using the principle of superposition, analysing the first and the second stages of operation, is obtained the static gain optimal total of the Double Quadratic Buck Converter proposed depending on the output voltage by the input voltage, given in (3.4).

$$\frac{Vc}{Vin} = D^2 \qquad (3.4)$$

Based on Equation(3.3),thevoltageontheswitchS_1isgiven by the voltage source in the upper input (V_{in}/2) added the voltage on the intermediate capacitor C_1 (V_C/2). Thus we have:

$$V_{s1} = \frac{Vin}{2} + \frac{Vc}{2} \qquad (3.5)$$

Considering the total input voltage V_{in} and also substituting V_C as a function of V_{in}, the voltage on the switch S_1 is obtained:

$$V_{s1} = \frac{3}{4}V_{in} \qquad (3.6)$$

The Equation (3.6) shows that the stress on the switch S_1 is small when compared to the Quadratic Buck Converter , and less than the total voltage at the input (V_{in}). The voltage on the switch S_2 is obtained similarly.

IV. SIMULATION AND RESULTS

4.1. Introduction

This chapter includes the simulation of Double Quadratic Buck Converter. The simulation of this converter is done by using MATLAB2010. The focus was on the output voltage of the converter and the voltage across the switches.

In this section , the closed loop simulation results of the Double Quadratic Buck Converter presented. The Table shows the values used in the simulation of the converter. The simulation of the converter was performed on the software MATLAB2010. The Fig. 4.2 shows the voltage on the output capacitor and Fig.4.2 shows the voltage across the switches S1 and S2, for the continuous conduction mode. The ripple voltage at the output is designed to be 1% of the average output voltage. This result shows the voltage at the switches is less than the input voltage set at 400V. The inductor current is an important parameter for determining the mode of operation of the converter. The ripple current in the inductor is designed to 10% of the total current, in continuous conduction mode.

4.2 Design

The analysis of a double quadratic buck converter is carried out on the basis of the following assumptions

Input voltage, V_{in} = 400V
Output Power, P_{out} =500W
Output Voltage, V_{out} = 100V
Switching frequency f_s= 50KH_z
Duty cycle = 50%
From equation (3.3)

· $\frac{V_c}{V_{in}} = D$

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Intermediate capacitor voltage $V_c = DV_{in}$
= 0.5×400 =200V
Equation for change in current

$$\Delta I_{L1} = \frac{V_{in}/2}{L_1} \times \frac{D(1-D)}{f_s} \qquad (4.1)$$

From equation (4.1), $L_1 = \frac{V_{in}/2}{\Delta I_{L1}} \times \frac{D(1-D)}{f_s}$

$$= \frac{200}{.25} \times \frac{.25}{50\times10^3} = 4\times10^{-3}$$

$L_1 = L_4 = 4$ mH

Equation for current through inductor L_2

$$\Delta I_{L2} = \frac{V_c/2}{L_2} \times \frac{D(1-D)}{f_s} \qquad (4.2)$$

From equation (4.1), $L_2 = \frac{V_c/2}{\Delta I_{L2}} \times \frac{D(1-D)}{f_s}$

$$= \frac{100}{.5} \times \frac{.25}{50\times10^3} = 1\times10^{-3}$$

$L_2 = L_3 = 1$ mH

4.3. MATLAB/Simulink model of double quadratic buck converter

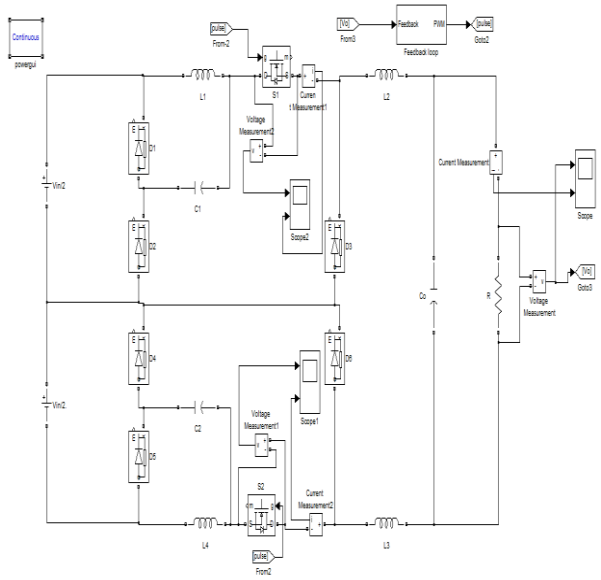

Fig.4.1.Closed loop Simulink model of double quadratic buck converter

4.4. Simulation results

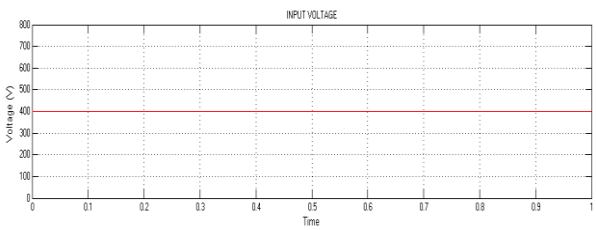

Fig.4.2. input voltage

4.4.1 Output Voltage with comparison

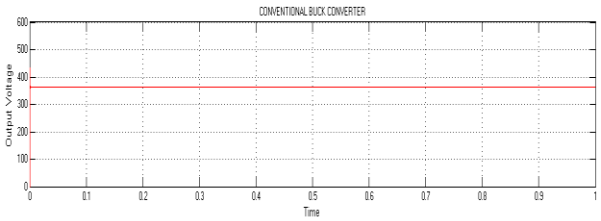

Fig.4.3. output voltage of conventional buck converter

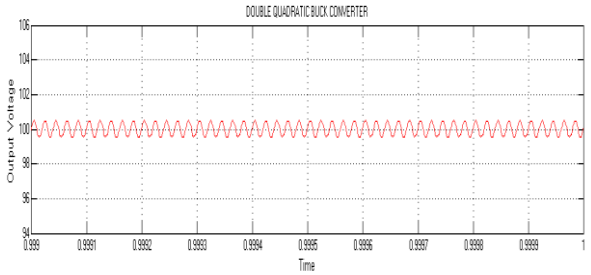

Fig.4.4. output voltage of double quadratic buck converter

CONVERTER	OUTPUT VOLTAGE
Conventional Buck Converter	100V
Double Quadratic Buck Converter	360V

Table.4.1. output Voltage Comparison

Simulation results are presented for continuous conduction mode and show the low value in the output voltage over the input value, proving the high conversion rate of the converter. Thus we can see double quadratic buck converter has the advantages of high gain rationearhalfrangeofdutycyclecomparedtotheconventional BuckConverter. The input 400V reduced to 100V.

4.4.2 Voltage across Switches with comparison

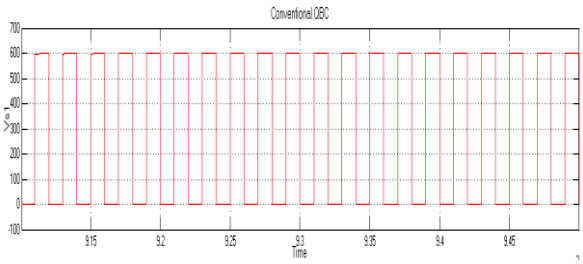

Fig.4.5. Conventional Quadratic Buck Converter

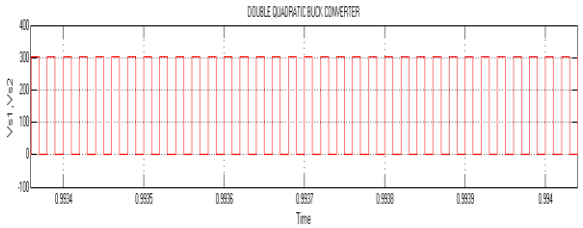

Fig.4.6. Double Quadratic Buck Converter

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CONVERTER	VOLTAGE STRESS OVER SWITCH
Conventional Quadratic Buck Converter	600V
Double Quadratic Buck Converter	300V

Table.4.2. Comparison of voltage stresses

In double quadratic buck converter, the stress voltage over the switches is reduced to half of the value compared to the conventional Quadratic Buck Converter.

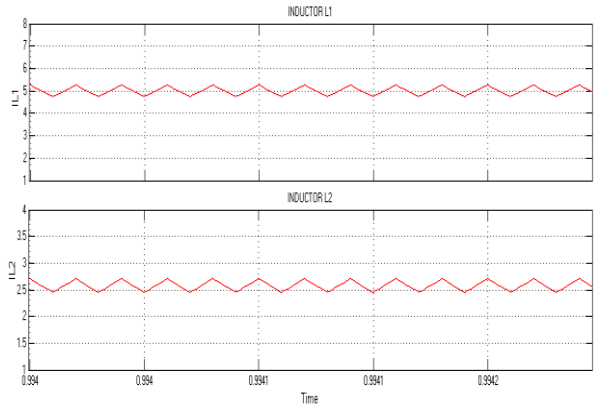

Fig.4.7.Inductor currents

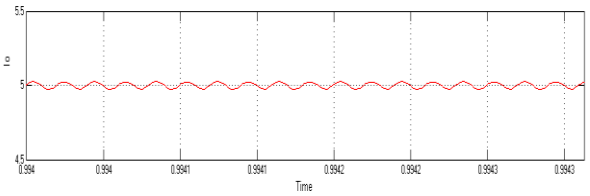

Fig.4.8.Output Current

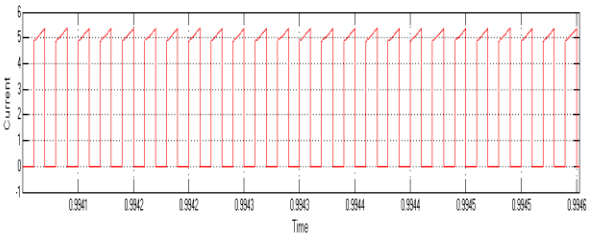

Fig.4.9.Current through the switches

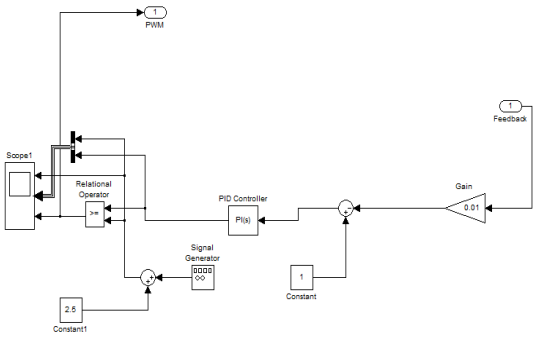

Fig.4.10. Control Loop

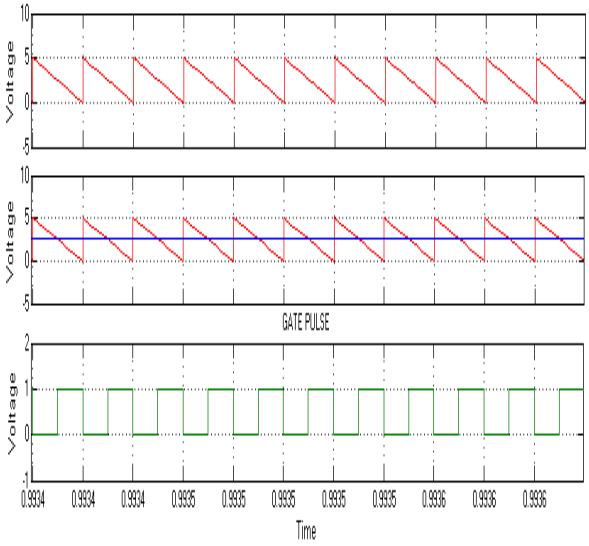

Fig.4.11. Generated Gate Pulse

4.5 Scale Down

For the implementation of hardware in laboratory the values are reduced. The input voltage is given as 24V for an output of 6V. The design and simulation with new values are given.

4.5.1 Design

The analysis of a double quadratic buck converter is carried out on the basis of the following assumptions

Input voltage, V_{in} = 24V
Output Voltage, V_{out} = 6V
Switching frequency f_s= 50KH_z
Duty cycle = 50%
From equation (3.3) $\frac{V_c}{V_{in}} = D$
Intermediate capacitor voltage $V_c = DV_{in}$

Equation for change in current

$$\Delta I_{L1} = \frac{V_{in}/2}{L_1} \times \frac{D(1-D)}{f_s} \qquad (4.1)$$

From equation (4.1), $L_1 = \frac{V_{in}/2}{\Delta I_{L1}} \times \frac{D(1-D)}{f_s}$

$$= \frac{12}{.25} \times \frac{.25}{50\times10^3} = .24\times10^{-3}$$

$L_1 = L_4 = .24$ mH

Equation for current through inductor L_2

$$\Delta I_{L2} = \frac{V_c/2}{L_2} \times \frac{D(1-D)}{f_s} \qquad (4.2)$$

From equation (4.1), $L_2 = \frac{V_c/2}{\Delta I_{L2}} \times \frac{D(1-D)}{f_s}$

$$= \frac{6}{.5} \times \frac{.25}{50\times10^3} = 0.06\times10^{-3}$$

$L_2 = L_3 = 0.06$ mH

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4.5.2 Simulink Model

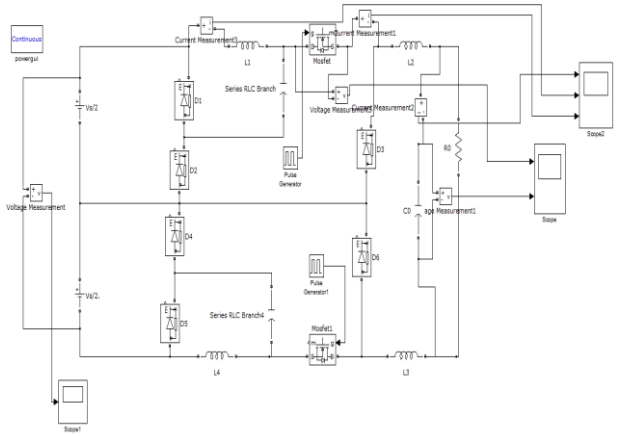

Fig.4.12. Scale Down Simulink Model

4.5.3 Simulation Results

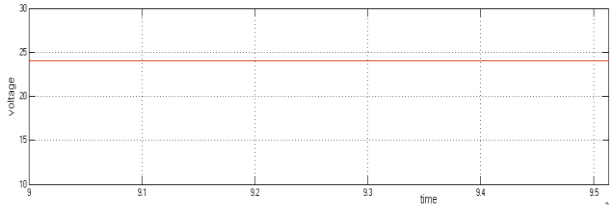

Fig.4.13. Input Voltage

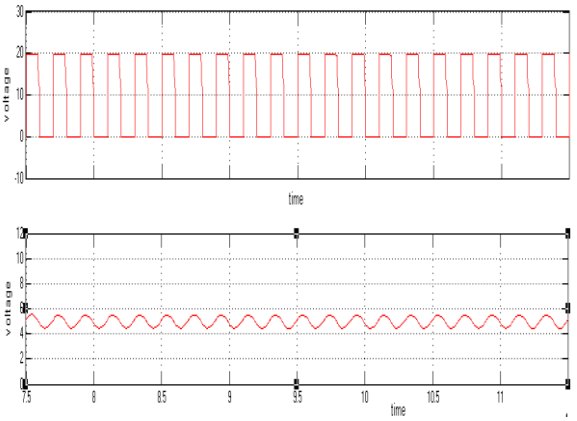

Fig.4.14. Voltage Across Switch And Output Voltage

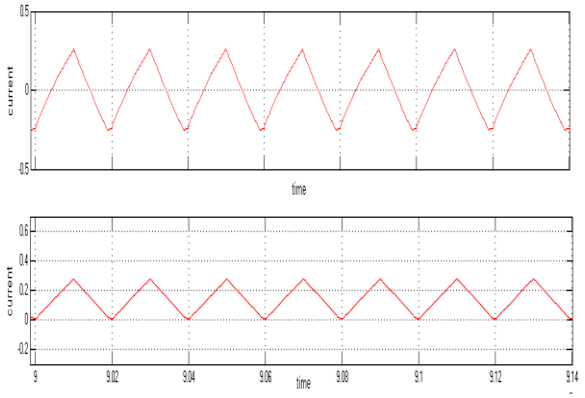

Fig.4.15. Inductor Currents L_1 and L_2

4.6Conclusion

The measured waveforms of the voltage across output capacitor and voltage across switches are shown in Figures. These voltage waveforms agreed with the operating principles and the comparison results with conventional converters. The current through various components of the circuit and the output current are also shown.

V. CONCLUSION

The study of a new Converter non isolated DC-DC step down Double Quadratic Buck Converter was presented in this paper. The topology of the converter, the stages of operation was presented. Simulation results are presented for continuous conduction mode and show the low value in the output voltage over the input value, proving the high conversion rate of the converter. Furthermore, because of its symmetry the voltage stressintheswitchesS1 andS2 are identical. The hardware and the simulation results of the converter were presented. Thus it will be possible to use this new converter in various applications such as the generation of photovoltaic energy, micro-grids, electric vehicles and others.

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